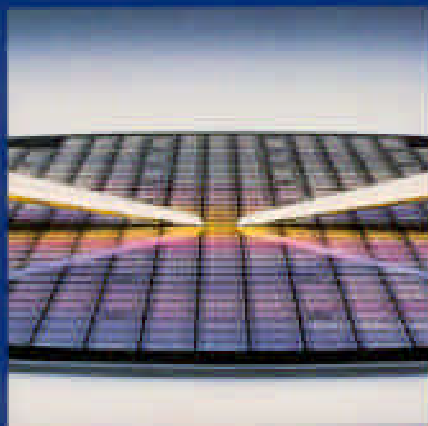
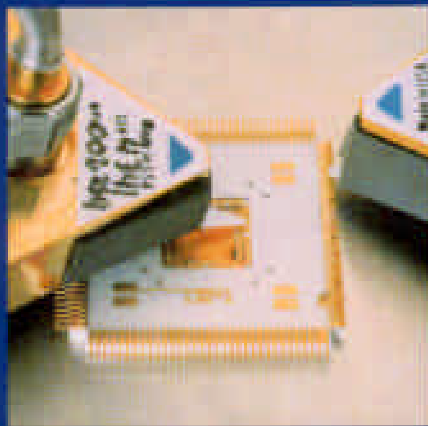
High Speed Digital Microprobing

Principles and Applications





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Introduction

The silicon digital integrated circuit (IC) industry is now poised on the edge of a major transition. The inexorable increase in speed brings unexpected problems related to high frequency operation. Edge rates of 0.5 nanoseconds off die, and 100 picoseconds on die are now common. What is unexpected is that digital ICs are affected by the same phenomena as microwave engineers are experiencing: ground plane resonances, skin effect, and antenna effects, to name a few. These phenomena, while difficult to model and predict with conventional digital circuit modeling tools, can be easily understood by looking at how the electric and magnetic fields are distributed.

This brochure provides a historical perspective, describing the underlying philosophy and assumptions of how digital circuits are currently understood, modeled, and measured. Because edge rates and circuit speeds are so high and continuing to increase, engineers are now entering a regime in which the previous underlying assumptions about digital signal conduction are no longer valid. Distributed models for both passive and active devices will be required to accurately predict IC performance on die, in the package, and in the PCB (printed circuit board) environment. Accurate high frequency models require accurate high frequency measurements. The traditional methods of measuring no longer consistently provide valid data for modeling. However, measurement techniques and equipment from the microwave industry have been adapted for the digital IC industry and are described for the following applications: packages, devices, ICs, and interconnects on ICs and PCBs.

Historical Perspective

Most engineers use circuit theory, assuming it will always accurately represent electrical phenomena. So, where did circuit theory come from and what are its underlying assumptions?

Ancient History

Back in the mid-l800s, Faraday and Gauss were discovering that there were forces between electric charges, and that moving electric charges would generate a magnetic field. Then it was discovered that a changing magnetic field would influence an electric charge, They developed the concept of electric and magnetic fields to model these effects. Maxwell put this all together into what are known as Maxwell's equations.

One of the solutions to Maxwell's equations is an infinite plane electromagnetic wave, with the electric field pointing only in the x direction and the magnetic field pointing only in the y direction, and the wave traveling in the z direction (Figure la), The propagation velocity is the speed of light, and the impedance is the ratio of the electric field to the magnetic field values or 377 ohms for free space.

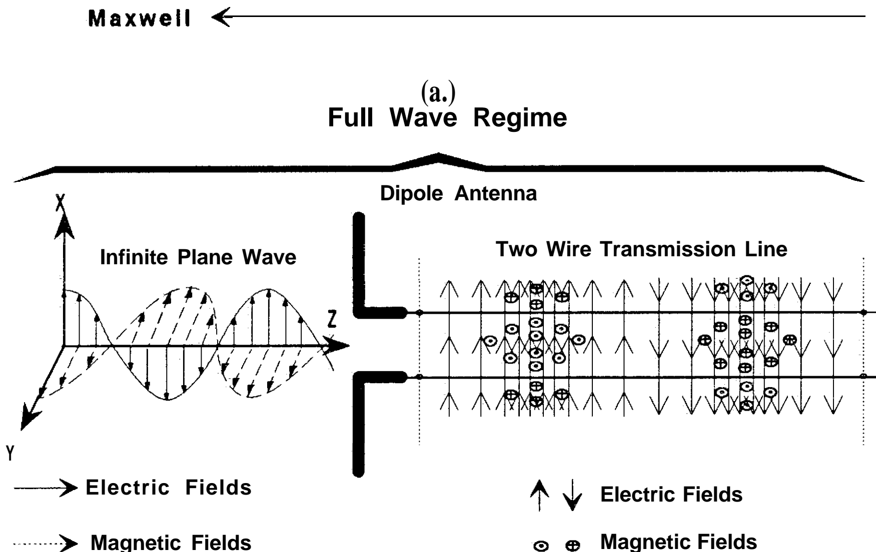
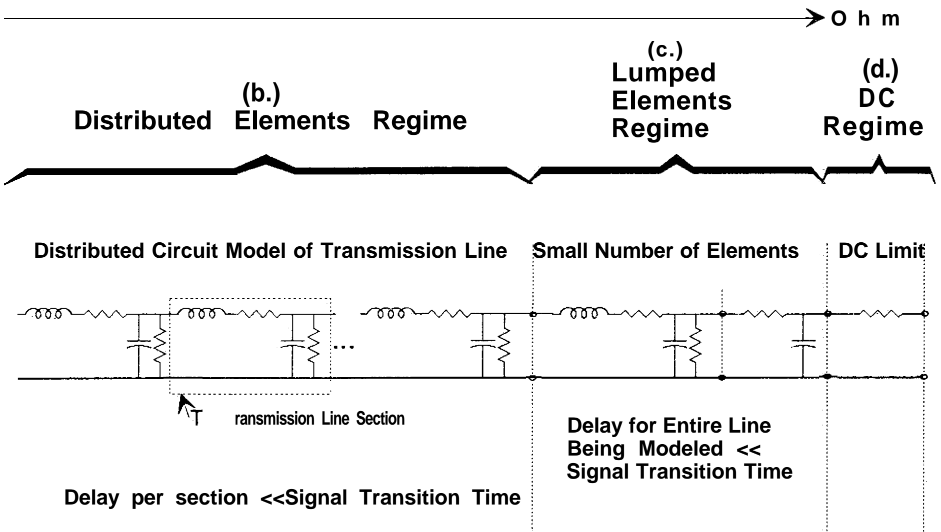


Figure 1. Analytical perspective illustrating the modeling progression from (a) Maxwell's equations, (b) distributed circuit elements, (c) lumped circuit elements, to (d) dc circuit assumptions.

When this plane wave encounters highly conductive objects, the direction of propagation changes. If the right shape is chosen, part of the plane wave can be diverted into a transmission line (Figure la). A transmission line is generally nothing more than the selective use of conductive materials to guide electromagnetic waves (Figure la). This is the Full Wave Regime, in which the application of Maxwell's equations are solved with boundary conditions selected to represent the physical dimensions and materials used. *All* circuits can be solved this way, and transmission line effects can be accurately predicted from this method.

The problem is that solving Maxwell's equations is difficult even for simple structures, so engineers have gone ahead and solved them once for simple structures, and then invented the concept of circuit theory to represent these solutions. They also made a number of assumptions to make circuit theory much more mathematically tractable than Maxwell's equations. And that is where the problem lies-we *use circuit theory and forget the assumptions.*

To simplify the mathematics, engineers decided to use capacitors to model the electric energy, inductors to model the magnetic energy, and resistors to model energy lost as heat.[1] These elements were defined to have zero physical size and were interconnected by wires with zero loss and zero delay.[2] By using these circuit elements, transmission lines could be modeled



without using Maxwell's equations and boundary conditions for each situation. The basic transmission line section is shown in Figure lb. Ideally, there are an infinite number of sections. However, for computational purposes (particularly for time domain solutions) a finite number of sections are used. The underlying assumption is the delay per section is much less than the signal wavelength or the signal risetime. Note also, that this transmission line model does not predict skin effect or dispersion, whereas solving Maxwell's equations would. Nor does circuit theory help someone design a transition from a coaxial transmission line to a microstrip transmission line, whereas the full wave theory would. This is the Distributed Element Regime, where electromagnetic waves are modeled by distributed circuit elements.

If the transmission line delay to be modeled is very short compared to the rise time, then a one section transmission line model will suffice, or even just an RC model (Figure 1c). This is the Lumped Element Regime, where the wavelengths of the electromagnetic waves being modeled are much larger than the circuit physical size, so a few small circuit element lumps will accurately model performance. And as the DC Regime is approached, just a resistor or zero delay wire will generally predict the performance with minimal error (Figure 1d).

The bottom line is that no modeling regime is right or wrong, rather it is important that you, the engineer, be aware of which regime your circuits will operate in and choose models and measurement tools appropriately.

Recent History

Figure 2 shows how gate propagation delays in the digital IC industry have decreased during the previous 20 years. There is every reason to believe that this trend will continue with ultra-high speed silicon processes being developed, having f_ts in the 75 GHz range.[3] Edge transition times on die are in the 100 ps range for fast ECL, and in the 0.5 ns range going off die through the package and the

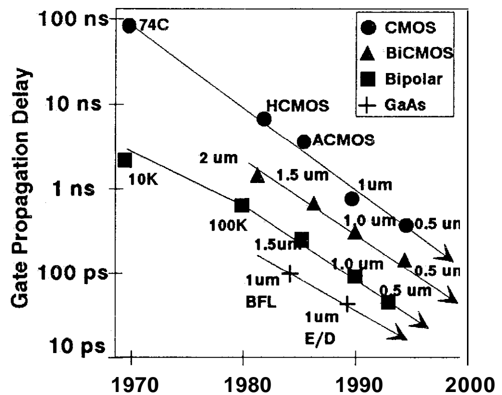


Figure 2. Historical progression of digital gate propagation delays.

PCB (printed circuit board). GaAs ICs are even faster, with off die transition times on the order of 100 ps.[4] ACMOS is capable of 1 ns edges, depending on loading.

Clock speeds are equally impressive. According to a Dataquest survey, 50% of all digital PC boards will run at higher than 50 MHz by 1991.[5] ECL and GaAs gate arrays typically operate at 200-500 MHz clock speed for large arrays and up to 3.5 GHz for small arrays.[6]

Figure 3 shows how digital elements have been historically understood and modeled. The earliest devices were very slow and could be modeled as gain elements. Interconnections on die could be ignored. Packages and PC boards were just wires or traces, which possessed no delay, no loss, and no capacitive or inductive parasitics. This approach corresponds to the DC Regime, where all parasitics and transmission line effects are ignored.

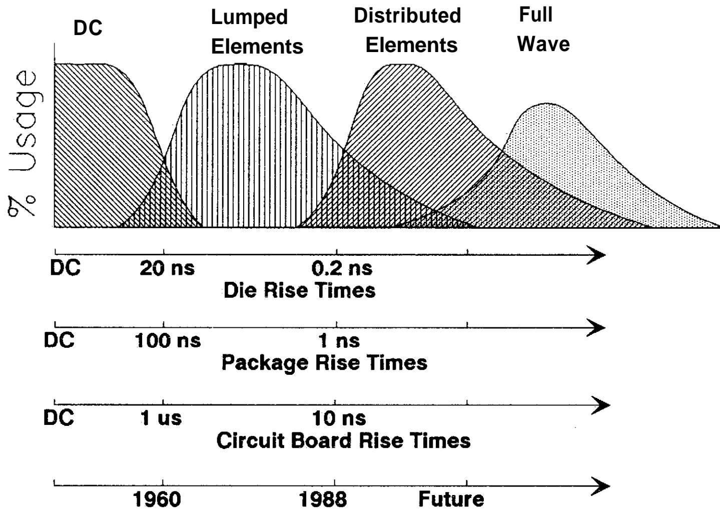


Figure 3. Historical progression of digital IC modeling methodologies.

As speeds increased, engineers very quickly noticed that devices contained Miller capacitances, and the diode isolation capacitances needed to be modeled. Interconnects on die had capacitive and resistive parasitics which affected rise times. Packages also had capacitive and inductive parasitics that affected rise times and could be measured with LCZ bridges or predicted with computer programs.[7] Worse yet, the ground reference in these packages was connected to the PC board ground by an inductor (the common-ground inductance of the package), resulting in ground bounce. PC board traces also

had capacitive and inductive parasitics. However, one could model and predict performance by adding additional circuit elements into the basic model. This is the Lumped Element Regime (Figure 3), where interconnects have zero delay, and all parasitics are modeled as lumped elements of zero physical size. This approach has worked very well during the last 20 years.

Because the longest interconnects are on backplanes and PC boards, the engineers designing and testing them first noticed a radical departure from circuit theory. At fast speeds, the longer traces exhibited transmission line behavior: ringing, overshoot, and reflections. This is the Distributed Element Regime (Figure 3), where signals generate both electric and magnetic fields that propagate at finite velocity. These effects are modeled by distributing the parasitic elements, effectively predicting the propagation velocity and other effects referred to as transmission line effects. Packaging designers are now entering this regime, and IC designers soon will follow.' Devices, when measured at high frequencies, also appear to be more accurately modeled with some of the parasitics distributed rather than lumped.

Beyond the distributed regime is the Full Wave Regime, where the electric and magnetic field distributions are obtained by solving Maxwell's equations for specific boundary conditions. While any circuit can be solved by Maxwell's equations, this approach is generally not practical. It is useful to package designers, for example, to use Maxwell's equations to analyze potential package designs because circuit theory generally will not predict antenna effects, ground plane resonances, and skin effect. Skin effect and dispersion will be discussed in more detail later.

Table 1 summarizes the characteristics and underlying assumptions of each of the modeling regimes. One of the more interesting aspects is how the energy flow is modeled. In circuit theory, lumped or distributed, the energy flow is modeled as positive electron flow, is contained by the wires, and is dissipated in resistive elements. The typical analogy is water flowing in a pipe. From Maxwell's equations however, the energy flow is in the electric and magnetic fields guided by the conductors and is converted to heat when the fields are incident on lossy dielectrics or conductors. In other words *the energy-flows in the gaps around the conductors and NOT in the conductors.* The impact, of course, is that at high frequencies the spaces between conductors are as important to signal conduction as the conductors themselves.

Modeled Elements	DC	Lumped Elements	Distributed Elements	Full Wave
Transmission Lines	Zero delay, Series R	1 RLC section	Multiple RLC sections	Electric & magnetic fields solved
Ground Planes	Zero delay, Series R	RC Circuit	2D distributed RLC circuit	Electric & magnetic fields, antenna/resonator
-Parasitics	Series R only	Lumped RLC	Distributed RLC	Implicit in solution
-Energy Flow	Electron flow in wires	Electron flow in wires, storage in L & C, dissipation in R	Electron flow in wires	Electric & magnetic fields in dielectric
-Skin effect	Not modeled	Not modeled	Partly modeled	Modeled
-Dispersion	Not modeled	Not modeled	Partly modeled	Modeled
Assumptions	Total delay < < < transition time, 0 delay wires, point source elements	Total delay << transition time, 0 delay wires, point source elements	Total delay < (transition time)/8,0 delay wires, point source elements	None
Active device models	No LC parasitics, dc data only	1 dimension models, lumped parasitics, dc data, 1 MHz ac data	2 dimension models, dc and 1 MHz ac data, ac data > f_t in frequency	2 & 3 dimension models, dc and 1 MHz ac data > f_t in frequency, antennas for radiation

Table 1. Summary and underlying assumptions of digital PC modeling methodologies.

Guidelines

So, when does the circuit begin to operate in the distributed regime? The basic guidelines are that distributed effects will begin to occur in interconnects when: [10]

$$L = \frac{T_r \times V_p}{8}$$

where L = interconnect line physical length
Tr = transition time in seconds
V_P = propagation velocity

$$V_p \approx c/(\varepsilon_r)^{1/2}$$

where c = speed of Light = 3×10^8 m/sec
ε_r = relative dielectric constant
= 1 for free space
≈ 4.9 for FR4 PCB material
≈ 10 for alumina
≈ 3.3 for polyimide

Ringing and other undesirable effects will occur when:

$$L = \frac{T_r \times V_p}{2}$$

if the interconnect is not modeled as a transmission line.[7]

For example, given a 1 ns transition time signal on a PC board (typical $V_P \approx$ 13 cm/ns), transmission line effects will begin with a 1.6 cm long trace, and big problems occur when the length is 6.5 cm or longer.

The impact of these guidelines is different for the on-die, the package, and the PCB environments because each is physically sized differently with respect to the wavelength of the frequency components present. As Figure 3 shows, each of these environments will encounter transmission line effects at different signal transition times.

Real Transmission Lines

Practical transmission lines for digital IC, package, and PCB use are shown in Figure 4. These transmission lines function similarly to the two wire example in that they guide electromagnetic waves through the selective use of conductive material. Microstrip (Figure 4a) is the most often used transmission line configuration in digital applications. It consists of a rectangular conductor situated over a conducting plane, separated by a dielectric material. Note that the electric fields are both in the air and in the dielectric. A variation of microstrip is stripline (Figure 4b), which has conducting planes above and below the center conductor. Stripline is commonly used in multilayer PC boards and complex packages. A less popular, but very useful configuration is coplanar waveguide (Figure 4c). Because of assembly and fabrication constraints, it is useful to have all conductors on the same plane.

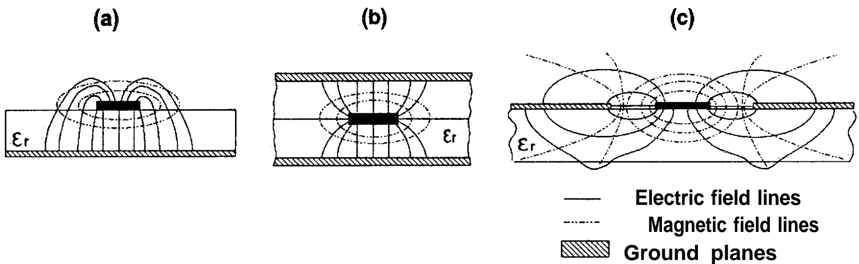


Figure 4. Practical transmission lines for digital use. Shown are (a) microstrip, (b) stripline, and (c) coplanar transmission line construction useful for digital ICs, packages, and PCBs.

Microstrip on silicon presents a whole new set of problems, as silicon is affected by fields generated by the propagating signal. Figure 5 is a CV (capacitance-voltage) plot of an MOS (metal-oxide semiconductor) structure. [11] This structure is similar to a microstrip transmission line on silicon, except the oxide thickness is usually thicker for transmission line use. Figure 5 shows the CV response for several modes of operation: Low frequency where both the dc bias and ac measuring signal is varied slowly (10 Hz), high frequency where the bias is varied slowly and the ac signal varies rapidly (1 MHz), and deep depletion where both the bias and ac signals are varied rapidly. The point is that typical IC silicon has electrical properties

that vary with local fields, so it makes a poor dielectric plane for a transmission line. Some work has been done in this area, however, much more investigation is needed. [12]

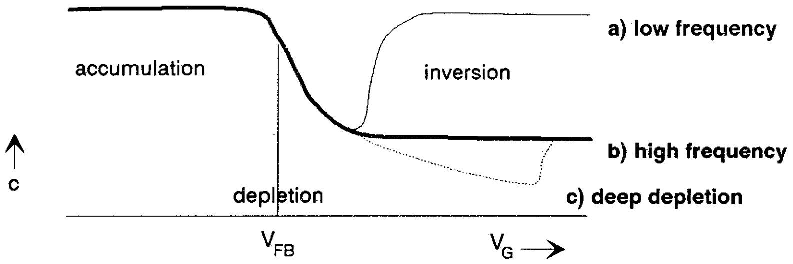


Figure 5. CV plot of a MOS structure, showing several models of measurement: (a) low frequency (10 Hz); (b) high frequency (1MHz); and (c) deep depletion.

Real transmission lines have losses due to (a) resistive losses in the conductor and (b) losses in the dielectric. Typical values are shown in Figure 6 for microstrip. [13] Note that silicon dielectric losses are the highest, and this is for a substrate of 1000 ohm-cm, not what is typically used. At this time, direct measurements are the only way of assessing transmission line loss on silicon substrates.

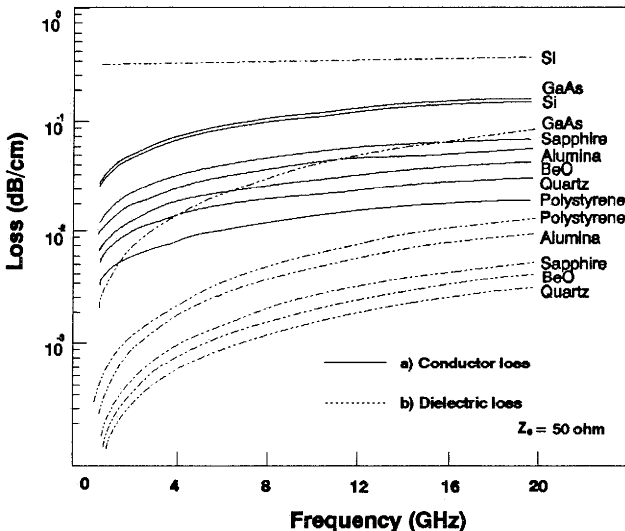


Figure 6. Typical microstrip losses for (a) losses in the conductor and (b) losses in the dielectric.

Unexpected Transmission Line Behavior

When a uniform plane electromagnetic wave (Figure 1) impinges on a good conductor, the time-varying fields attenuate very quickly within the conductor. The magnitude of the electric field and the resultant current density attenuates as:

$$J = \sigma E e^{-z\sqrt{\pi f \mu \sigma}}$$

where
J = current density
E = electric field strength
σ = conductivity
f = frequency of incident electromagnetic wave
μ = magnetic permeability of the conductor

The result is that as the electromagnetic wave frequency increases, the induced current in the conductor retreats to the surface. The currents flows in a skin at the surface of the conductor, and this is termed *skin effect.* The current density decreases as l/e into the conductor (Figure 7). The distance to where the current density equals l/e = 0.368 of the value at the surface of the conductor is termed the *skin depth.*

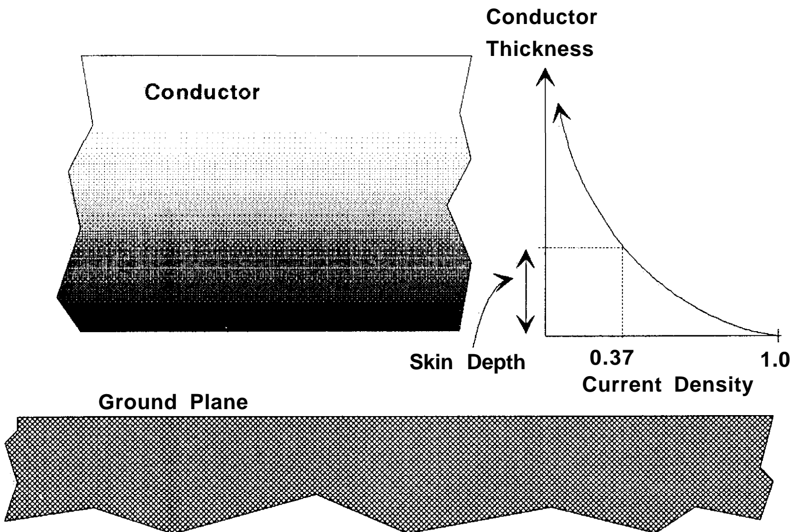


Figure 7. As the frequency increases, the current density is more concentrated at the surface of the conductor (skin effect). The current density decreases exponentially with distance from the surface.

Or $$\Delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

where
Δ = skin depth in meters
σ = conductivity
f = frequency
μ = magnetic permeability

For copper this reduces to:

$$\Delta = \frac{0.06661}{\sqrt{f}}$$

where
Δ = skin depth in meters
f = frequency

At 1 GHz, the skin depth in copper is 2.1 μm

For aluminum

$$\Delta = \frac{0.0826}{\sqrt{f}}$$

The impact of skin effect on the time domain response is complex, but if several simplifications are made, one arrives at the following expression, with the input signal being a step function. [14]

$$V(t) = V_0\left\{1 - erf\sqrt{\frac{\tau}{t - T_0}}\right\}$$

where
t is time
V_0 = amplitude of incident step function
T_0 = time delay of transmission line
erf = error function

Tau (τ) is related to the attenuation coefficient of the line and the square of the line length.

A typical response is shown in Figure 8. Note that the 10-50% transition occurs in 4τ, but the 10-90% transition takes approximately 120τ. This can be understood intuitively by recalling the Fourier expansion of a step function. Because the skin depth is less at higher frequencies, the higher frequency components are attenuated more, resulting in the rolled-off response. Note

this expression is greatly simplified and is not expected to represent the response of real microstrip and coplanar lines, for example. At this time, direct measurement is the only way to accurately assess the skin effect of arbitrary structures.

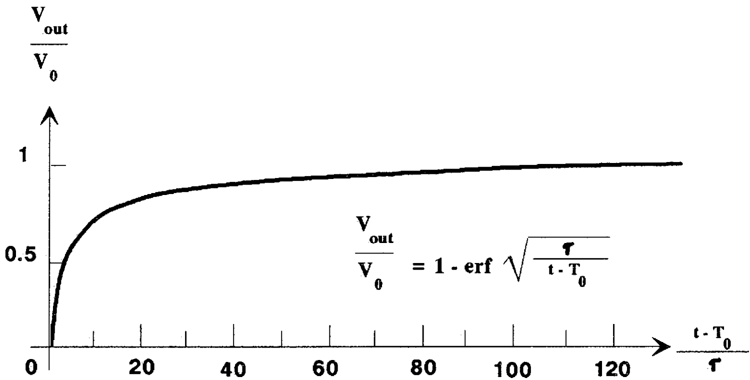


Figure 8. Typical degradation of step input due to skin effect. Incident waveform is a unit step function.

The guideline is that skin effect will have an impact on conductor loss when the conductor cross sectional dimensions are twice the skin depth at a particular frequency. The rise time degradation because of skin effect is proportional to the square of the transmission line length, Very short lines, such as short interconnects on ICs, are not likely to exhibit skin effects. The skin depth for aluminum at 1 GHz is 2.6 μm, and 0.83 μm at 10 GHz. These dimensions are larger than the typical metalization thickness (0.2 μm) so that skin effect will not be as important as other factors, unless thick metalization is used. The situations is different, however, on PCBs and backplanes, where the conductors are thicker and longer, and where skin effect will be important at high speeds.[15]

Dispersion

Some transmission lines exhibit a change in propagation velocity with frequency. Typically, higher frequency components of a waveform travel more slowly than lower frequency components. Again, recalling the Fourier expansion of a square wave (see Appendix-Bandwidth Requirements), the effect of dispersion will delay the higher frequency components, smearing the original waveform. An example is shown in Figure 9, using a Gaussian pulse for computational convenience.[16] Note how the waveform distorts as it moves down the microstrip line. It is expected that dispersion becomes

apparent when the signal wavelength (or about 5 transition times) is comparable to the cross sectional dimensions of the conductors. This implies that dispersion will be important only on the longer transmission lines on PCBs and cables and only with the fastest edges currently used.

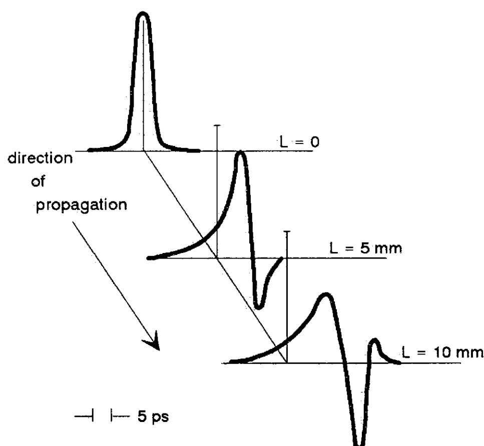


Figure 9. Example of dispersion of a Gaussian pulse as it travels along a microstrip line.

Impact

During the next 5 years, interconnect and device modeling will change considerably. The biggest change will be in the interconnects, with SPICE-type distributed models becoming available for microstrip, coplanar, and stripline transmission lines. Device models will also undergo evolutionary change with the addition of distributed parasitic elements, more accurately modeling and predicting the high frequency behavior. Until then, direct test structure measurement is the only way to acquire believable data, particularly when working on the technology edge. Current circuit theory using lumped parasitic elements will certainly not predict high frequency performance. And solving Maxwell's equations is nearly intractable for any useful real structure. The recommendation is to make measurements of special test structures representative of the process, package, PCB, or whatever. Then, using the measured data, the current models can be patched, giving useful predicted performance until newer distributed models are developed and verified with numerous measurements.

High Frequency Measurement Techniques

Circuit theory takes on a mysterious quality when used to represent transmission lines, reflections, mismatches, transitions, and skin effect. However, using field representation makes these concepts easy to understand. To minimize reflections, the field patterns must closely match, and when they do not match very well (such as connecting coaxial to a microstrip), reflections can occur because the field pattern of coaxial does not match the field pattern of microstrip. The solution is also obvious. Simply design a tapered structure which provides a gradual transition from the radial coaxial fields to something approaching a microstrip field (Figure 10).

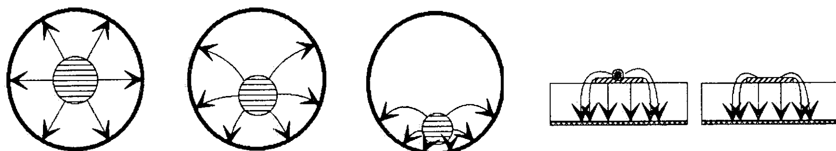


Figure 10. Details of a measurement grade coax to microstrip transition showing how the electric fields are gradually varied to achieve a good match.

The same principles apply to high frequency parameter measurements. The connection to the circuit under test must match the fields that are to be measured. Simply connecting a big scope probe to the circuit under test and using the typical ground wire is no longer acceptable. Instead, probes provide transmission lines all the way to the probe tips (Figure 11), designed to match fields from the DUT (device under test) through the coaxial connector all the way to the scope, TDR, or network analyzer. These probes are currently the most accurate way of guiding high frequency waves onto

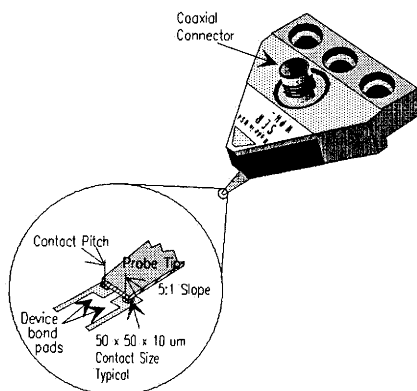


Figure 11. Details of Cascade Microtech coplanar high frequency probes.

and off a die, package, or PCB. Needle probes, soldered-on SMA connectors, or coaxial probes can be used, but they all have a poor field match to the DUT, resulting in poor repeatability (10-30%) and poor accuracy.

When used with automatic network analyzers (ANA), such as the Hewlett-Packard 8510 Series for example, (Figure 12), and time domain reflectometers (TDR) such as the Hewlett-Packard 54121T (Figure 13), the

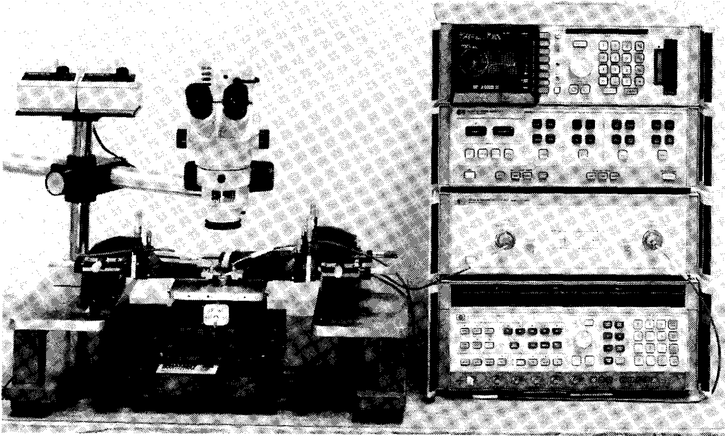


Figure 12. The HP 8510 Series Network Analyzer, used in conjunction with the Cascade Microtech Summit 9000™ Analytical Probe Station and high frequency probes, can make precision measurements of devices, packages, and interconnects.

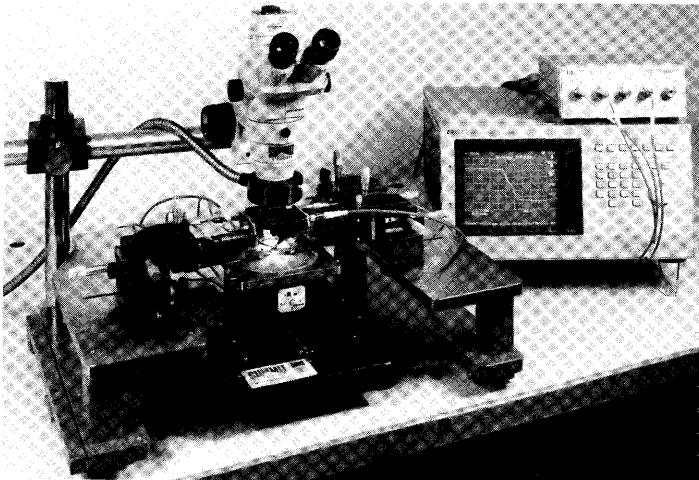


Figure 13. The HP 54121T TDR and digitizing scope in conjunction with Cascade Microtech Summit 9000 probe station and coplanar probes. By using external calibration elements, TDR equipment can achieve accurate high speed measurements.

probe and cable response can be calibrated out by using the Impedance Standard Substrate (ISS) made by Cascade Microtech (Figure 14). This substrate contains various precision elements, including 0.3% resistors,

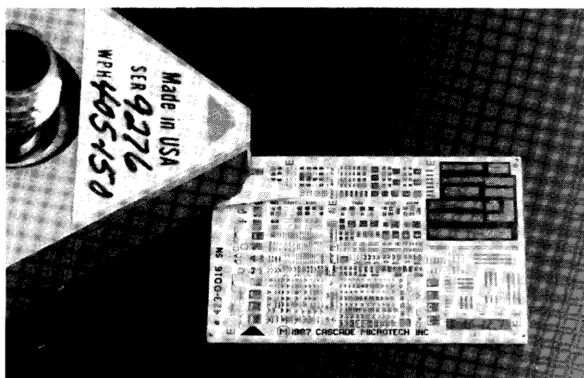


Figure 14. Cascade Microtech probe landing on an Impedance Standard Substrate (ISS) used for calibration before measurement.

transmission lines, shorts, and throughs necessary to calibrate the measurement system up to the probe tips. A typical calibration sequence is shown in Figure 15. After calibration, the measurement system will measure only what is beyond the probe tips. Coplanar probes, with effective calibration, accurately set the measurement reference plane at the probe tips.

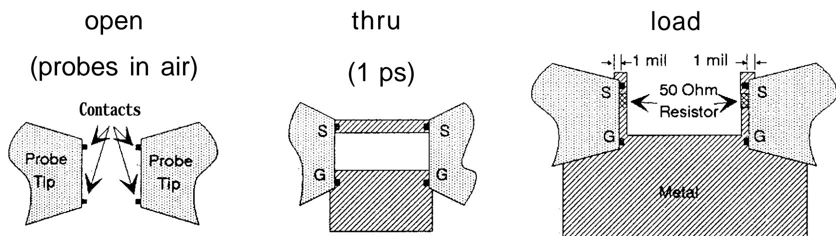


Figure 15. Typical calibration sequence using a HP 8510 network analyzer, Cascade Microtech probes, and ISS.

S-parameters

The units of high frequency measurements are different than those for lower frequency measurements. At low frequencies arbitrary circuit networks are often characterized by their H, Y, or Z parameters. The measurement of these parameters requires the placement of short and open circuits on the network ports. The use of shorts and opens at high frequencies presents several problems. At high frequencies, accurate shorts and opens are difficult to obtain because of parasitic electrical circuit elements. Also, active devices are often not stable with opens or shorts because of internal device parasitic electrical elements. To get around these problems, engineers measure scattering parameters (S-parameters), which typically require 50 ohm terminations. It is much easier to get a good 50 ohm termination at high frequency than a good short or open, and active devices are usually stable with 50 ohms.

S-parameters are based on traveling power wave reflections or scattering, where there is an incident traveling wave and a reflected traveling wave. For a one-port network, there is only one S-parameter.

$$S_{11} = b_1/a_1$$

where
b_1 is the reflected power wave from the input port
a_1 is the incident power wave toward the output port

In other words, S_{11} is simply the ratio of reflected energy to the incident energy. This is very similar to how a TDR (time domain reflectometer) functions, where a voltage step is incident on a network and a portion of the incident voltage wave is reflected depending on the network. The TDR reflection coefficient ρ is then

$$\rho = v_2/v_1$$

where
v_1 is the incident voltage wave
v_2 is the reflected voltage wave

Measurements of S-parameters and TDR response are fundamentally similar. S_{11} is normally expressed as a reflection magnitude and angle at a particular frequency. A TDR-derived ρ is expressed as magnitude at a particular point in time or distance, assuming a specific propagation velocity. The biggest practical difference is that S-parameters can be used to develop a quantitative model, whereas TDR data generally provides qualitative data.

Note that the above discussion of one-port parameters can easily be expanded to two and more ports.

To summarize, the measurement equipment and techniques must match the modeling regime applicable to the circuit and application (Table 2).

Regime ⇒	DC	Lumped Elements	Distributed Elements	Full Wave
Equipment	dc V&I system	dc V&I system, 1 MHz LCZ meter, 1 MHz CV meter	dc V&I system, 1 MHz LCZ meter, 1 MHz CV meter, network analyzer, TDR	dc V&I system, 1 MHz LCZ meter, 1 MHz CV meter, network analyzer, TDR, radiation measurement equipment
Connections to the DUT	Wires, simple probes, alligator clips	Coaxial cables & probes, soldered coaxial connectors, needles, probe cards	Cascade Microtech probes (providing transmission lines to the DUT)	Cascade Microtech probes (providing transmission lines to the DUT), antennas, receivers

Table 2. Equipment requirements for the four modeling regimes.

Package Measurements

Digital LSI and VLSI packages are now required to operate at clock rates of 50-250 MHz and beyond. This requires analog bandwidths of 500-2500 MHz for good edge definition (see Appendix A for a discussion of how analog bandwidth relates to digital bandwidth). At these frequencies, typical digital packages will exhibit electrical behavior completely unpredicted from low frequency measurements and models. Complicating the issue, typical digital packages have metal pattern dimensions that resonate and/or couple to the outside environment-they can act as antennas and resonators. This is the microwave domain, where open lines may appear as short circuits and shorted lines as opens, depending on the frequency. Microwave designers have been successfully working with these issues for years, and now these techniques have been adapted to the high speed digital design environment.

A first-order equivalent circuit of a digital IC package is shown in Figure 16. The common-ground inductance models both ground bounce and the

induced common lead crosstalk. The lossy transmission lines will model reflections, losses, and other distributed effects while lumped capacitors and mutual inductors model cross coupling between adjacent signal traces.

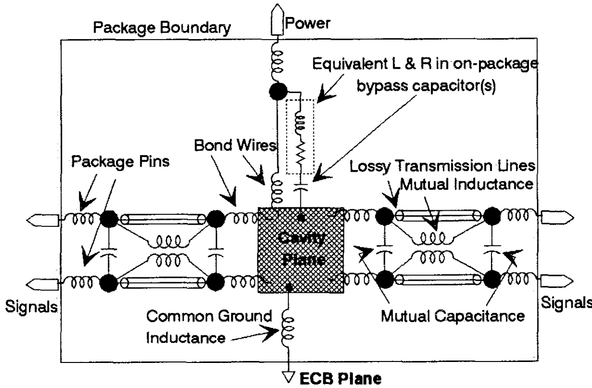


Figure 16. First order equivalent circuit of a digital IC package.

Contacting a complex package requires an interface fixture such as a Surrogate Chip™ test substrate, which is mounted in a cavity, wire bonded to the traces under test, and probed with either standard Cascade Microtech probes or Cascade Microtech steep-angle package probes (Figure 17).

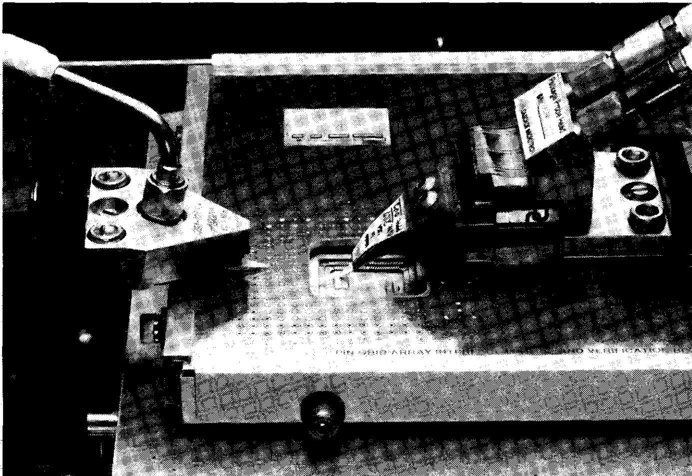


Figure 17. Surrogate Chip™ test substrate contacted by Cascade Microtech steep-angle package probe.

Another effective way is to mount the package under test to a specially designed circuit board with pads for high frequency probes, as shown in Figure 18. Package test fixtures and boards are available from Cascade Microtech.

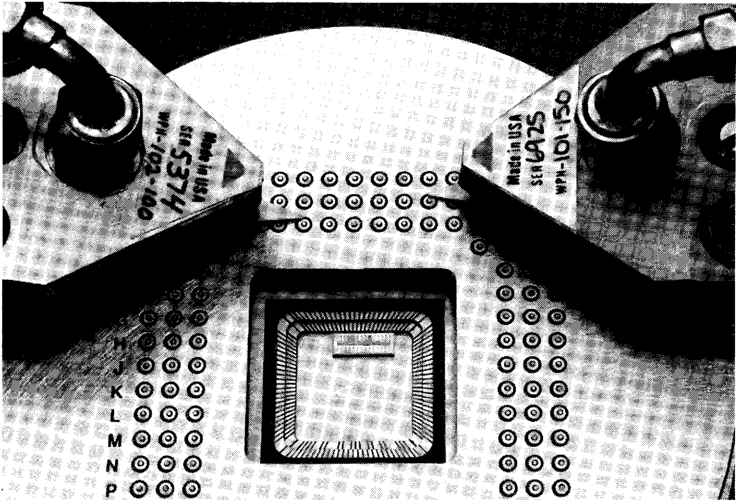


Figure 18. Cascade Microtech's package test fixture with 169 PGA attached. Probes contact the desired pins by contacting the circular land and the adjoining ground.

Figure 19 is an example of TDR data of the longest, shortest, and two additional signal traces of a 169 PGA that are open circuited in the cavity.

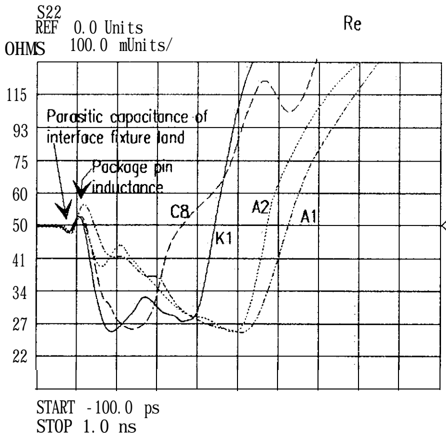


Figure 19. TDR of the longest (A1), shortest (C8), and two additional signal traces in a 169 PGA. The traces are not terminated in the cavity.

Ground inductance is common to all measurements and is one of the most difficult parameters to measure accurately. Figure 20 shows the Smith chart results of a typical common-ground inductance measurement. Recall that on a Smith chart, all purely resistive values lie on the horizontal axis, with (in this case) 50 ohms in the center, 0 ohms on the far left, and infinite ohms on the far right. Inductive responses are on the top semicircle, and capacitive on the bottom. The frequency response of a pure inductor starts at the far left (a short circuit) at dc, and as the frequency increases, travels clockwise around the top of the Smith chart, until finally, at infinite frequency, it is at the far right point.

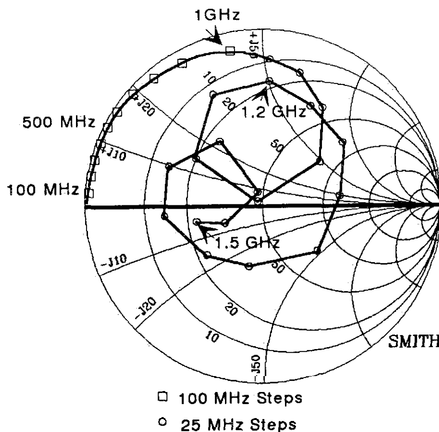


Figure 20. Smith chart response of ground inductance measurement. Note initial inductive response, followed by three closely spaced (in frequency) resonances (looping).

The S-parameter data (Figure 20) shows an inductive response through 1.1 GHz, with a small resistive component (indicated by the response moving towards the center of the Smith chart). Various resonances are then encountered, shown by the looping on the Smith chart. Where the data crosses the horizontal axis, the input impedance is a pure resistance. At the frequency where it approaches the center of the Smith chart, the impedance is 50 ohms and terminates the input perfectly; all the signal is absorbed.

Ground plane resonance is a fundamental performance limit of a package. What occurs at resonance is that the plane is no longer an equipotential, but rather acting like an antenna, radiating to the dielectric and to all signal traces on the package. Given that this resonance occurs at ≈ 1 GHz, and using the analog-to-digital bandwidth rule of thumb of 10:1, this would imply

a maximum clock rate for this package of 100 MHz, *for ground plane resonance limitations only.*

Device Measurements

Until recently, device modeling engineers either extrapolated low frequency data, or diced, packaged, fixtured, and measured individual die to obtain f_t and other high frequency parameters such as SPICE parameters for base transit time and excess phase. Both of these methods are fraught with errors which increase as the f_t to be measured increases. The first method is faulty because extrapolation has been shown to be invalid.[17] When using the second method, the response of the fixture, package, and bond wires must be de-embedded from the measured response. With Cascade Microtech high frequency probes now available, one simply needs to lay out appropriate test structures, contact them with probes, and measure.

When measuring minimum-size devices, such as 2 x 9 µm or smaller emitter sizes, the capacitive parasitics associated with the bond pads are as large as the device values (Figure 21), resulting in significant error.

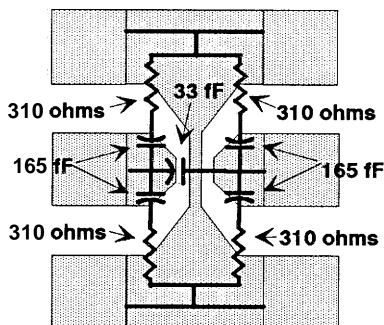


Figure 21. Parasitic values associated with typical device pad-out structures.

The recommended technique is to include a "dummy device" (Figure 22), which is just an open set of pads.[18]

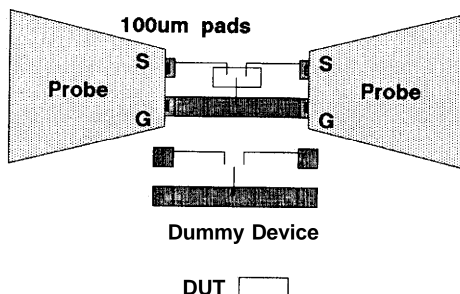


Figure 22. Recommended layout for high frequency probing (≈ 26 GHz) of test devices, including "dummy device" used to correct for pad-out parasitics.

The measurement sequence then becomes:

1. Calibrate the entire measurement system to the probe tips.

2. Measure S-parameters of the dummy device.
    a. Convert S-Parameters to Y-parameters, store data.

3. Measure DUT S-parameters
    a. Convert S-parameters to Y-parameters
    b. Subtract dummy Y-parameters from DUT Y-parameters
    c. Convert back to S-parameters, or H-parameters as desired, store data.

4. Repeat step 2 for each DUT surrounding the dummy.

Typical results for a 2 x 3 μm emitter device are shown in Figure 23. Note that even for a 3 GHz device, ignoring the effect of the pads results in almost 50% error in f_t.

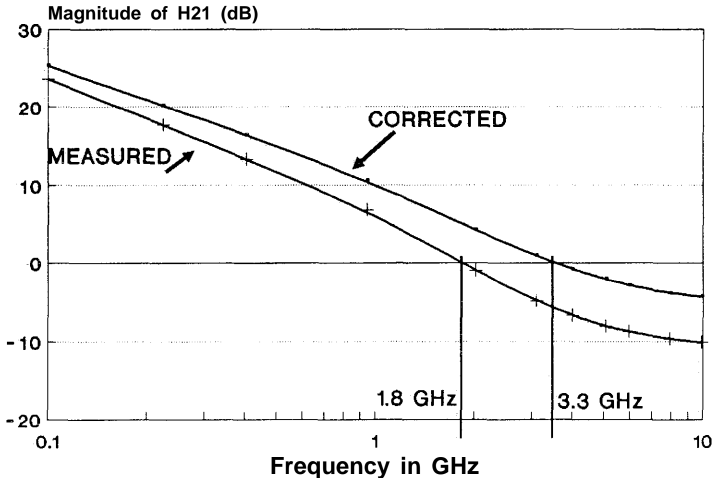


Figure 23. H_{21} plot of a 2 x 3 μm emitter transistor showing the effect of correcting for pad parasitics on f_t.

IC Measurements

Many digital ICs have several high speed inputs and outputs. If the total number of pads is 44 or less, the Cascade Microtech WPH-700 series multicontact probes can be used to probe an entire IC on the wafer at speed (Figure 24).

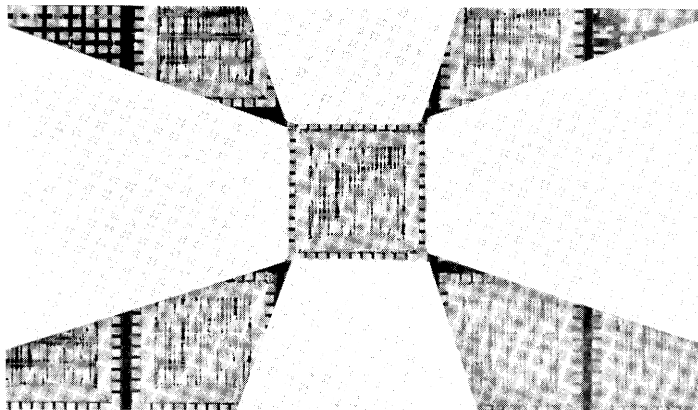
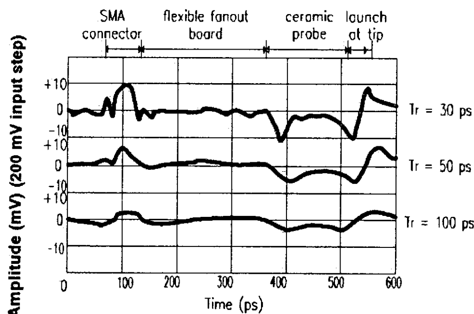


Figure 24. Cascade Microtech WPH-700 series multicontact probes contacting a high speed MUX die during high-speed wafer sort.

These probes function well with 30 ps risetimes (Figure 25).

Figure 25. TDR response of a Cascade Microtech multicontact probe with 30, 50, and 100 ps risetime.



Each of the contacts is factory programmable to function as either a:

- unterminated signal line
- signal line terminated in 50 ohms to ground
- signal line terminated in 50 ohms to V_{ref}
- ground line
- power bypass line
- no contact

The power bypass option provides high quality bypassed power to the IC under test. This is particularly important if the IC has high di/dt requirements. The characteristics of the bypassed power contact are shown in Figure 26. Many relatively low speed ICs with 10-50 MHz clock rates have large 1 ns current spikes on power supply contacts.

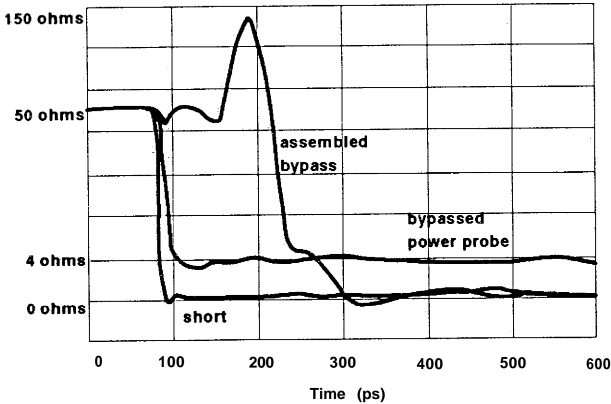


Figure 26. TDR of a short, an assembled bypass circuit, and the WPH-700 bypass circuit.

Larger die with more pads currently require a different strategy. By selectively locating the high speed contacts together, the multicontact probes can be combined with low frequency needle probes to make a mixed-signal probe card, as shown in Figure 27.

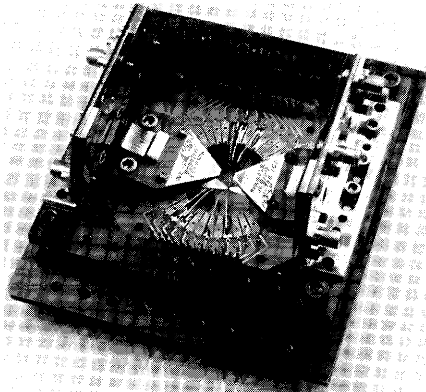


Figure 27, Cascade Microtech WPH-700 multicontact probes in a probe card with dc needle probes.

Binning static RAMs (random access memory) is a typical application where the fastest RAMs are put into faster, more expensive packages and the slower ones into standard DIPs (dual in-line packages). Obviously, it would be impossible to package and then test, so bin-testing at speed and binning on-wafer is required. A few tenths of nanosecond ringing could be expensive in this situation.

Interconnect Measurements

Interconnects are likely to be the limiting factor on speed in the 1990s, so careful characterization and modeling is going to be important. Careful characterization begins with careful test structure layout, and this is where field theory is most helpful. The key to a good layout is to replicate the field pattern that will actually occur in the real IC, or package, or PCB. When thinking of interconnects in this manner, their underlying complexity becomes apparent. Simplifications will need to be made; merely go a step at a time when adding complexity.

In general, the interconnects being measured are expected to be representative of interconnects which do not have pads, so the technique to remove the pad response described above can be used successfully. Typical interconnect test structures are shown in Figure 28, for microstrip, and coplanar transmission lines.

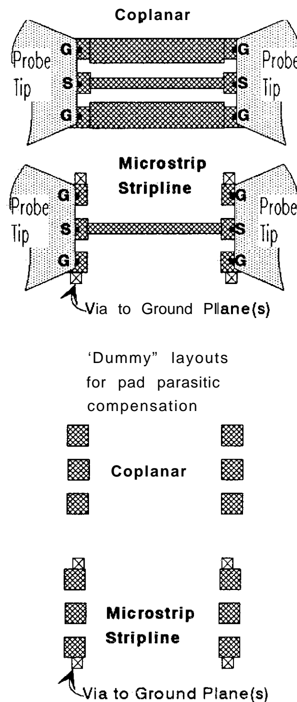


Figure 28. Typical test structure for high frequency measurements of interconnect transmission lines.

An example result is shown in Figure 29 for a 50 ohm microstrip line on 0.062 inch thick FR4 PCB material. The line is 1.5 inches long.

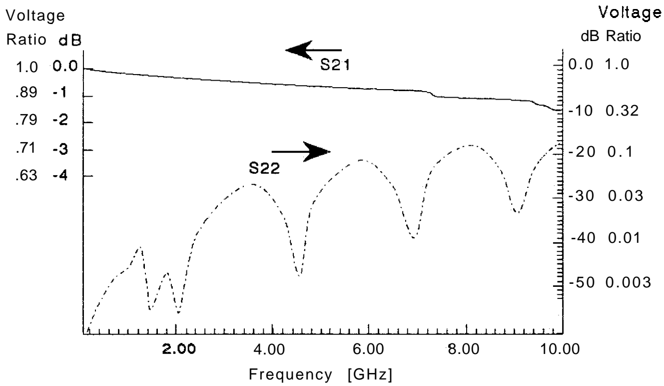


Figure 29. Response of 1.5 inch microstrip line on verification board. S21 is the transmission loss and S22 is the reflected energy.

Propagation velocity and end effects can be seen by obtaining TDR measurements of different length open (or shorted, or terminated) lines as shown in Figure 30.

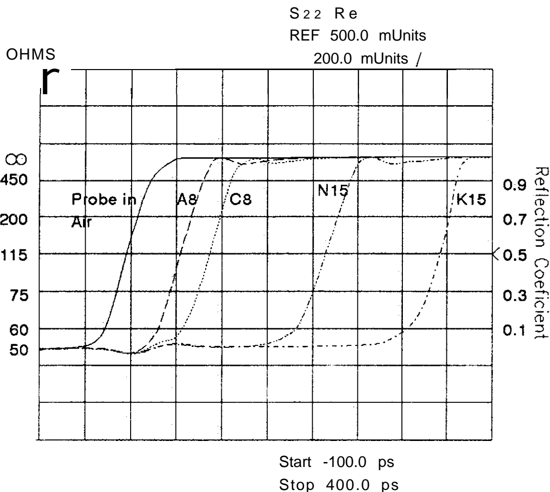


Figure 30. TDR response of several open microstrip lines on 0.062 inch FR4.

Interconnects on silicon are a special case, as the response may be affected by the transition times and the amplitudes. This means that small signal measurements may not accurately predict large signal behavior, so that a TDR pulse of 200 mV may not mean anything when the real 5 V signal hits the line. Obviously, in this case, use actual signals. Try adding a large, variable dc bias to the small signals. If the line response changes with the dc bias change, then a non linear situation is evident. Actual signals are generally required for accurate measurements.

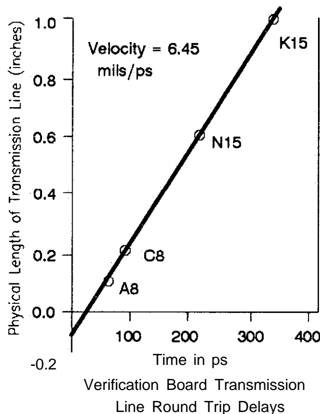


Figure 31. Plot of physical length vs. round trip delay of the lines measured in TDR from Figure 30. The propagation velocity is the slope of the line, corrected to a one-path delay. The Y-intercept is a measure of the end effects (fringing, etc.)

APPENDIX- Bandwidth Requirements

A common question when measuring devices is "How high in frequency should the device or package be measured at to assure a required digital performance ?" The most direct approach is to compute the Fourier expansion coefficients for a train of square waves and look at how each additional harmonic affects the risetime (Figure Al).

Risetime vs Harmonic content
100 MHz CLOCK

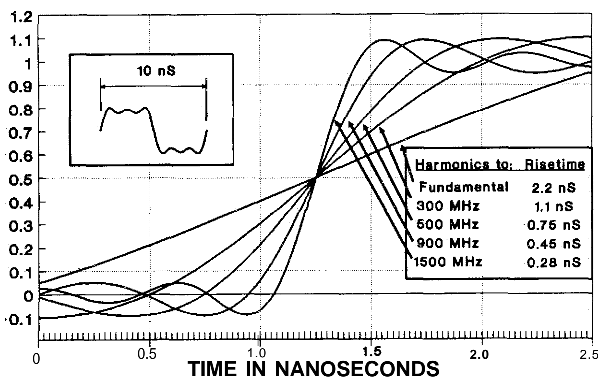


Figure A1. Risetime vs. harmonic content for a 100 MHz square wave.

This data can be linearly scaled for any arbitrary clock frequency shown in Figure A2. Note the assumptions here are (a) symmetric square wave clock, (b) and no phase shift as a function of frequency. In general, the expected risetime for a 100 MHz clock is about 0.5 ns, meaning that harmonic content to at least 900 MHz is required, and harmonic content to 1500 MHz would be desirable for a well defined edge.

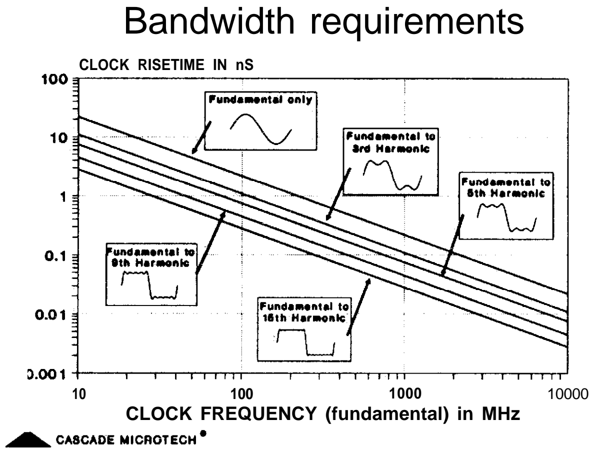


Figure A2. Bandwidth requirements for risetime performance, assuming square waves.

The general guideline is that a square wave clock requires harmonics to 10 times the fundamental clock frequency. For package characterization purposes, use an analog bandwidth of 30 times the maximum expected digital clock frequency. This recommendation corresponds well with the recommendations in MIL-STD-883[19]. This extended bandwidth will allow exploration of various resonances, and an assessment of how much margin the package has, and will result in more accurate package models. Keep these guidelines in mind when selecting equipment, including network analyzers, cables, probes, and other fixtures. Figure Al is also useful to estimate maximum signal risetimes, given that the maximum analog bandwidth of a package is known, When using Figure Al, keep in mind the above assumptions; if they are violated, the estimated risetimes for a given bandwidth will go down.

Contributors

Arthur Fraser is the Applications Manager at Cascade Microtech.

Keith Jones is the Engineering Manager at Cascade Microtech.

Ed Godshalk is a Microwave Design Engineer at Cascade Microtech,

Bob Hickey is a Research Engineer at Cascade Microtech.

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